CLAIMS

1. A method of manufacturing a source-gated transistor, including:

(a) providing a transparent substrate (2);

(b) depositing a gate layer and patterning the gate layer to form a gate (4);

(c) depositing a gate insulating layer (6);

(d) depositing a thin film semiconductor layer (8);

(e) depositing a source layer (18) defining a barrier with the semiconductor layer (8), using a step of back exposure through the substrate using the gate (4) as a mask to define the barrier between source layer (18) and the semiconductor layer (8).

2. A method according to claim 1 further comprising:

defining a drain region (24) in the semiconductor layer in contact with a drain contact;

wherein spacers (28) are used to define the lateral extent of a spacer region (32) of the semiconductor layer (8) in registration with the gate (4) using a self-aligned process, the spacer region (32) being the region between the drain region (24) and the barrier.

3. A method according to claim 1 or 2 wherein the source layer is a transparent source layer, further including

(f) depositing photoresist (12,22) on the transparent source layer (18);

wherein the back exposure step includes exposing the photoresist by illumination through the substrate (2), gate insulator (6), semiconductor layer (8) and transparent source layer (18) using the gate (4) as a mask.

4. A method according to any preceding claim further comprising defining a field relief region or regions (32,48) at the edge of the source in registration with the gate (4) using a self-aligned back exposure process in which the field

relief region or regions are patterned using photoresist on the top of the substrate exposed with illumination passing through the substrate (2) using the gate (4) as a mask.

5. A method according to any preceding claim including the steps after step (d) of

(e) depositing a transparent source layer (18) for forming a barrier at the interface between the transparent source layer (18) and the semiconductor layer (8);

(f) depositing a positive photoresist layer (22);

(g) exposing the positive photoresist layer (22) through the transparent substrate (2) and source layer (18) using the gate (4) as a mask to pattern the photoresist in self-alignment with the gate (4);

(h) etching the transparent source layer (18) to form a source region using the pattern defined directly or indirectly by the photoresist layer (22);

(i) forming spacers (28,36) at the edge of the source region either before, after or during step (h);

(j) implanting dopants into drain regions of the semiconductor layer (8) using the source region (18) and spacers (10,28) as a mask to form highly doped drain regions spaced from the source region by the width of the spacers.

6. A method according to claim 5 including:

depositing an insulating layer (10) after step (d) of the depositng the semiconductor layer (8);

etching the insulating layer (10) to form a source window (14) in alignment with the mask.

7. A method according to claim 5 or 6 further comprising:

depositing a transparent sacrifical layer (20) on the transparent source layer (18) before carrying out steps (f) and (g) of depositing and patterning the positive photoresist layer (22);

after carrying out step (g), forming spacers (28) on the sidewalls of the transparent sacrificial layer (20) so that the spacers (28) and transparent sacrificial layer (20) are together wider than the gate; and

using the transparent sacrificial layer (20) and spacers (28) as a mask to etch the source layer (18) and the underlying insulating layer (10) to leave the source layer extending over a region wider than the gate and to form the insulating layer to define a field plate spacer (10) between the source layer (18) and the semiconductor layer (8).

8. A method according to claim 5 wherein step (i) of forming spacers is carried out after the step (h) of forming the source region so that the spacers are formed on the edges of the source region.

9. A method according to any of claims 5 to 8 further comprising performing an implant into the semiconductor layer (8) after step (h) of forming the source region to form a doped region (32) of the semiconductor layer (8) in alignment with the source region (18).

10. A method according to any preceding claim further comprising depositing a barrier-lowering implant (16) in the semiconductor layer (8).

11. A method according to claim 10 wherein the barrier lowering implant is self-aligned to the gate but implanted over a narrower area than the area of the gate defining a field relief region (48) of the central region around the barrier lowering implant which is not implanted with the barrier lowering implant.

12. A method according to any preceding claim further comprising depositing a transparent insulating layer (42) in the central region at the centre of the barrier between the source (18) and semiconductor layer (8).

13. A transistor, comprising:

a transparent substrate (2);

a gate (4) on the substrate (2);

gate insulator (6) on the gate;

a semiconductor layer (8) over the gate;

a source (18) extending along the semiconductor layer (8) defining a barrier at the interface between source (18) and semiconductor layer (8) overlapping the gate (4);

a heavily doped drain region (24) of the semiconductor layer (8); and

self-aligned spacer regions (32) defining a lateral separation between the drain region (24) and the barrier.

14. A transistor according to claim 13 further comprising a barrier-lowering implant (16) in the semiconductor layer (8).

15. A transistor according to claim 14 wherein the barrier lowering implant is provided in the central part of the barrier defining a field relief region (48) of the central region around the barrier lowering implant.

16. A transistor according to any of claims 13, 14 or 15 further comprising a transparent insulating layer (42) in the central region at the centre of the barrier between the source (18) and semiconductor layer (8).